High-Q Factor Three-Dimensional Inductors

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***Abstract*—In this paper, the great flexibility of three-dimensional (3-D) monolithic-microwave integrated-circuit technology is used to improve the performance of on-chip inductors. A novel topology for high-Q factor spiral inductor that can be implemented in a single or multilevel configuration is proposed. Several inductors were fabricated on either silicon substrate ($\rho = 30\ \Omega \cdot$ cm) or semi-insulating gallium–arsenide substrate demonstrating, more particularly, for GaAs technology, the interest of the multilevel configuration. A 1.38-nH double-level 3-D inductor formed on an Si substrate exhibits a very high peak Q factor of 52.8 at 13.6 GHz and a self-resonant frequency as high as 24.7 GHz. Our 4.9-nH double-level GaAs 3-D inductor achieves a peak Q factor of 35.9 at 4.7 GHz and a self-resonant frequency of 8 GHz. For each technology, the performance limits of the proposed inductors in terms of quality factor are discussed. Guidelines for the optimum design of 3-D inductors are provided for Si and GaAs technologies.**

***Index Terms*—GaAs, high-Q factor, inductors, silicon, three-dimensional MMIC technology.**

I. Introduction

THE growth of commercial mobile wireless communication systems has raised the demand for multifunctional and highly integrated monolithic microwave integrated circuits (MMICs). Even if the issues are not the same, both silicon and GaAs MMICs require high-Q factor on-chip inductors.

For the future development of GaAs millimeter-wave wireless single-chip transceivers that can process low IF signals or baseband signals, the ability to realize highly integrated low-operation frequency devices is of particular interest. Below C-band, the use of lumped inductors greatly reduces circuit size compared to designs that use distributed matching elements. It results in a higher number of circuits per wafer, lower cost, and higher yield. The use of high-Q factor inductors improves circuit performance in terms of noise figure, insertion loss, gain, and power-added efficiency.

Silicon MMICs have two great advantages over GaAs MMICs, i.e., low process cost and possible integration with digital large-scale integrated (LSI) circuits, and, thus, provide all-silicon solutions for highly integrated transceivers. As regards conventional silicon integrated circuit (IC) designs using differential pairs, Gilbert cells or R–C coupled configuration, on-chip inductor-based designs enable lower supply voltages and offer higher operation frequencies and lower power dissipation. However, the inductor's quality factor degrades at high frequency due to the silicon substrate losses, and current silicon MMICs still have operation frequencies to the order of several gigahertz.

Therefore, for both silicon and GaAs technologies, enhancing the on-chip inductor's Q factor is an important task. The three-dimensional (3-D) MMIC technology formed either on silicon [1]–[3] or GaAs [4]–[6] substrates is an attractive solution to this common issue.

The 3-D process consists of four 2.5-μm-thick polyimide layers and five conductor layers whose thickness is 1 μm, except for the top conductor layer, which is 2-μm thick. The first four conductor layers from the top one are gold metallization layers. The bottom conductor layer at the interface between the 3-D process and the active process is formed with gold for the GaAs active process and aluminum for the silicon active process. All these conductor layers enable us to implement thin-film microstrip (TFMS) lines and inverted TFMS lines that can be interconnected by small via-holes though the dielectric layers. The ground can be formed on any of the five conductor layers, which offers a high flexibility of design.

The 3-D process is superimposed onto the silicon or GaAs active-device process (transistors, resistors, or capacitors) previously formed on the substrate. Compared to the conventional planar MMIC technology, the 3-D MMIC technology offers substantially higher integration levels [5], [8]. Eventually, the weak change in the active device's performance after the addition of the 10-μm-thick polyimide layer of the 3-D process [7] enables us to consider the 3-D MMIC technology for MMIC development. The 10-μm-thick polyimide layer also provides a good isolation of the passive devices on the top of the circuit from both the active devices and substrate.

In this paper, we propose a novel inductor topology that fully utilizes the potential of the 3-D MMIC technology. 3-D inductors implemented either in single-level or multilevel configuration on a silicon or GaAs substrate. The fabricated inductors exhibit enhanced performances due to the thick dielectric layer, ground plane that overlays the substrate, and low line losses. A fabricated 1.38-nH double-level spiral inductor based on silicon technology exhibits a very high peak Q factor of 52.8 at 13.6 GHz and a self-resonant frequency as high as 24.7 GHz. Our 4.9-nH double-level GaAs 3-D inductor achieves a peak Q factor of 35.9 at 4.7 GHz and a self-resonant frequency of 8 GHz. These results show that the 3-D MMIC technology is very effective in implementing high-performance silicon and GaAs inductors and, thus, provides the ability to realize high integrated single-chip transceivers.

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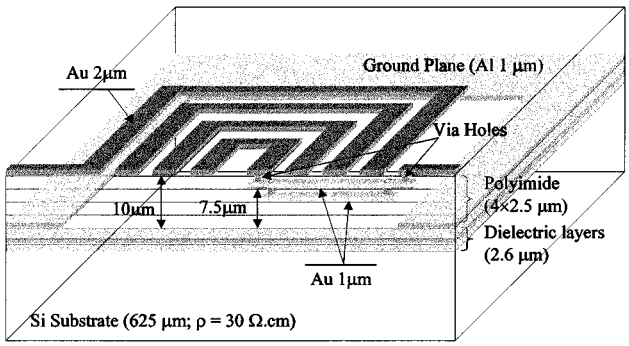

Fig. 1. Cross section of the proposed one-level conductor layer 3-D inductor fabricated using the silicon 3-D MMIC process.

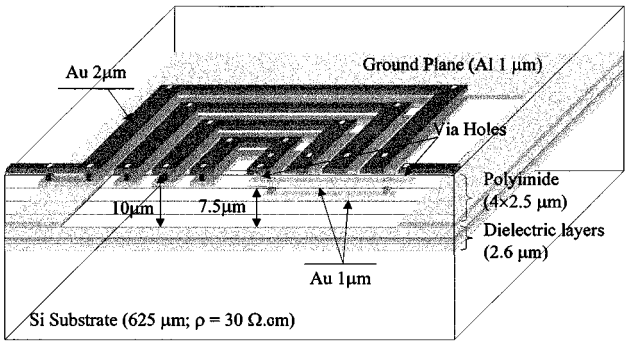

Fig. 2. Cross section of the proposed 3-D Si inductor in a two-level conductor layer configuration.

II. HIGH-Q FACTOR SILICON 3-D INDUCTORS

A. Introduction

Many approaches have already been reported to address the substrate issue of silicon on-chip inductors. Some of them use high-resistive silicon substrates [9], [10], thick dielectric layers [11] and/or thick conductor lines [12], multilayer conductors [13], [14], and recently, micromachining techniques [15], [16]. However, with the possible exception of the promising micromachining techniques, none of these techniques simultaneously achieve high inductance, high-Q factor, and high resonance frequency because they fail to completely offset the parasitic capacitance formed between the inductor spiral pattern and silicon substrate.

B. Basic Structure and Principle

Fig. 1 shows a cross section of the proposed 3-D inductor fabricated according to the 3-D process on conductive silicon substrate ($\rho = 30\ \Omega \cdot$ cm). The spiral pattern is formed on the 2-μm-thick top-level Au layer of the 3-D process to benefit from its low loss. Two 1-μm-thick TFMS lines located 2.5 and 5 μm under the spiral pattern are used to form a low-loss inductor underpass.

One innovative aspect of this inductor is the open ground plane formed on the lower-level Al layer of the 3-D process, 10 μm under the spiral pattern. Though the ground plane is open under the spiral pattern to provide high impedance inductor segments, its effect, combined with that of the 2.6-μm-thick dielectric (silicon–oxide/silicon–nitride/silicon–oxide) layer of the active process, substantially reduces the magnetically induced current (eddy current) in the Si substrate leading to low parasitic capacitance to the substrate.

Another important factor that minimizes the substrate effect is the thick (10 μm) polyimide layer of the 3-D process; it drastically reduces the losses of the TFMS line (>50% reduction) compared to the conventional coplanar line formed using the silicon process. Moreover, this thick dielectric layer prevents a drastic increase of the capacitance to the ground plane. The use of gold metallization instead of aluminum to fabricate the TFMS line of the spiral pattern contributes to a decrease in the inductor series losses.

Note that the use of the thick polyimide layers and open ground plane to provide isolation between the spiral pattern and silicon substrate makes the proposed 3-D inductor very similar to the coplanar inductor formed on a semi-insulated substrate.

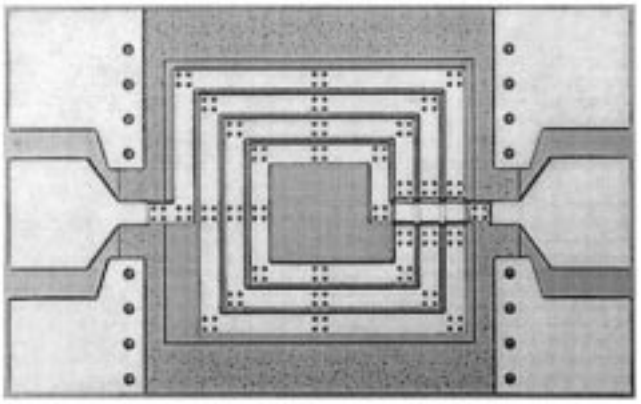

Fig. 3. Fabricated double-level three-turn inductor in silicon 3-D technology: $w = 20\ \mu$m, $G = 10\ \mu$m, $D = 100\ \mu$m with interconnection via-holes on the corners and center of the spiral segments.

C. Multilevel Configuration

A multilevel configuration 3-D inductor is also proposed, as shown in Fig. 2, for two levels of metal layer. The inductor is formed by two spiral patterns stacked on the top- and second-level conductor layers of the 3-D process. These two patterns are interconnected at regular positions by via-holes through the first dielectric layer (typically at the corners and middle of the inductor segments). The underpass of the inductor is still formed by two 1-μm-thick TFMS lines located on the second- and third-level conductor layers of the 3-D process so that an interruption is created on the bottom spiral pattern of the inductor.

D. Fabrication and Experimental Results

Fig. 3 shows an example of double-level 3-D Si inductors fabricated with a linewidth w of 20 μm and an internal diameter D of 100 μm. All the inductors were formed according to the 3-D process over an ordinary silicon active device's process (0.5-μm bipolar technology [17]). Most of the inductors were fabricated with a ground window that surrounds the spiral pattern with a gap G of 10 μm. The line-to-line spacing s is 5 μm and the conductive silicon substrate ($\rho = 30\ \Omega \cdot$ cm) is 625-μm thick. Additional double-level inductors were fabricated with interconnecting via-holes on all the spiral segments to compare with the proposed double-level configuration.

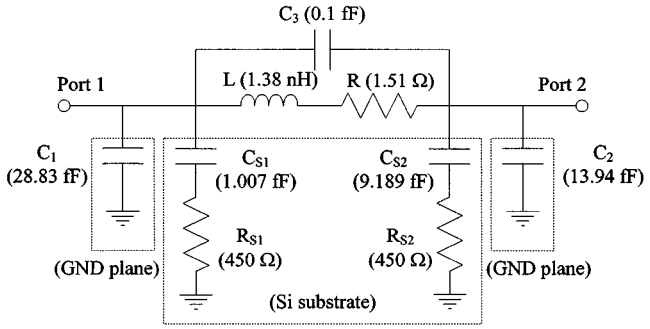

Fig. 4. Lumped-element equivalent circuit model of the 3-D silicon inductors and extracted elements for a 1.38-nH double-level fabricated inductor.

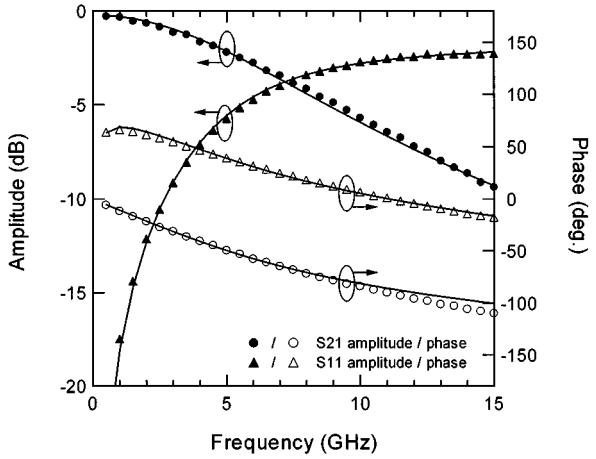

Fig. 5. Comparison between measurements and model of a four-turn $w = 20\ \mu$m 3-D silicon inductor ($L = 2.45$ nH).

The inductors were characterized on-wafer from 0.2 to 60 GHz, as well as open and short pad reference circuits for the device-under-test (DUT) RF pads to be deembedded. Fig. 4 shows the two-port lumped-element model of the 3-D silicon inductors. As shown in Fig. 5 for a 2.45-nH inductor ($n = 4$, $w = 20\ \mu$m), the model is in good agreement with the measurements. Eventually, Figs. 6–12 resume the fabricated inductors' charts based on this model and deduced from measurements. For all measurements, the silicon substrate resistance is found to be constant $R_{S1} = R_{S2} = 450\ \Omega$ and the feedback capacitance C_3 is 0.1 fF.

The inductance range for the fabricated 3-D inductors runs from 0.2 to 4.2 nH. As shown in Figs. 6 and 7, the inductance achieved with the double-level configuration is slightly decreased from that of the single-level configuration. This is partly due to the lower inductor self-inductance (related to the line characteristic impedance decreasing) and the increased negative mutual inductance. This effect is offset by an increase in the mutual inductance so that the total inductance of the double-level 3-D inductors remains high. We can see from Fig. 6 that the double-level inductors and double-level inductors with interconnecting via-holes on all the lines have almost identical inductance.

Fig. 8 shows the series resistance of the fabricated 3-D silicon inductors plotted versus the inductance. As expected, both for $w = 10\ \mu$m and $w = 20\ \mu$m, the series resistance of double-level inductors is effectively reduced compared to single-level inductors. This is in favor of an increase of the Q factor. Nevertheless, the proximity of the bottom spiral pattern to the ground and the conductive substrate increases the value of the parasitic capacitors (see Figs. 9–12).

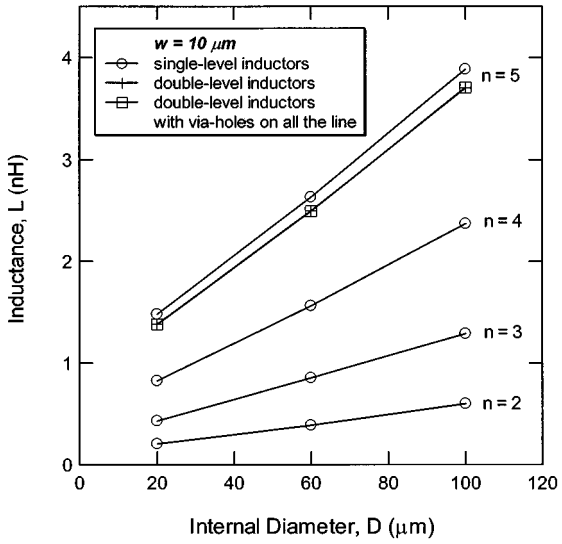

Fig. 6. Inductance chart of the fabricated $w = 10\ \mu$m 3-D silicon inductors.

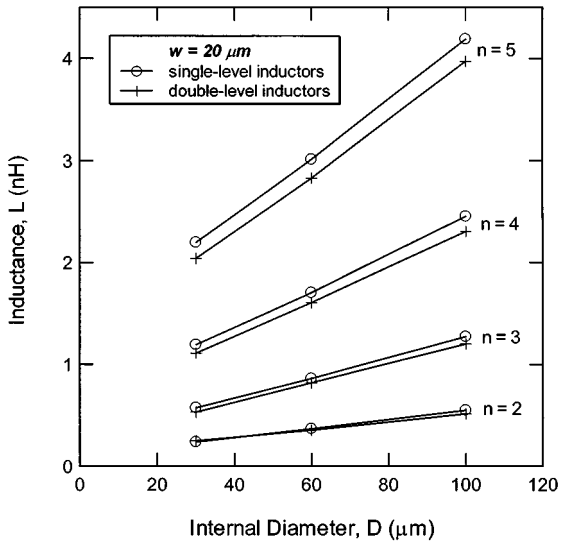

Fig. 7. Inductance chart of the fabricated $w = 20\ \mu$m 3-D silicon inductors.

Figs. 9–12 indicate that no significant change is seen in the parasitic capacitance between the double-level inductors and double-level inductors with via-holes on all the lines. Therefore, the Q factor is expected to be slightly higher for the latter configuration due to its lower series resistance.

Fig. 13 shows the peak Q factor of the fabricated 3-D silicon inductors versus the inductance. This value was deduced from the one-port S-parameter measurements of the inductor when an ideal short is placed at output port 2 (see Fig. 4). The Q factor was then calculated from the conventional equation

$$Q = \frac{\mathrm{Im}[Z_{\mathrm{in}}]}{\mathrm{Re}[Z_{\mathrm{in}}]} \tag{1}$$

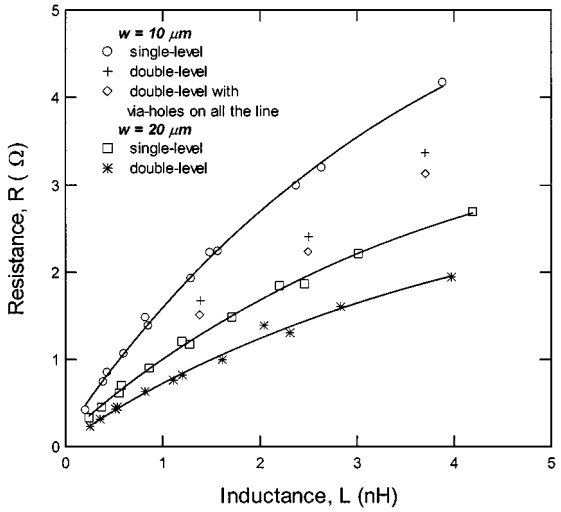

Fig. 8. Resistance versus inductance of the fabricated 3-D silicon inductors.

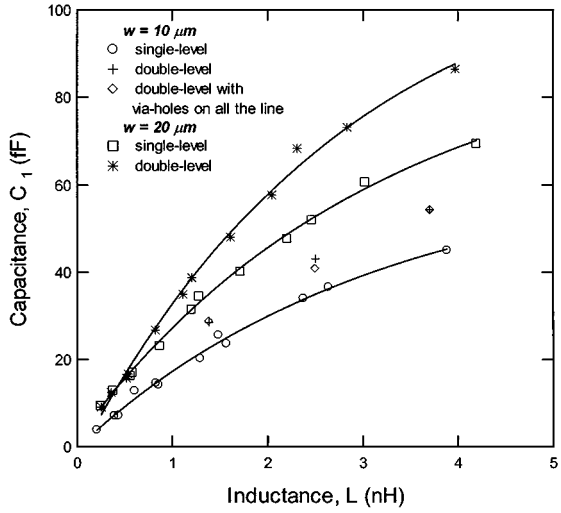

Fig. 9. Capacitance C_1 versus inductance of the fabricated 3-D silicon inductors.

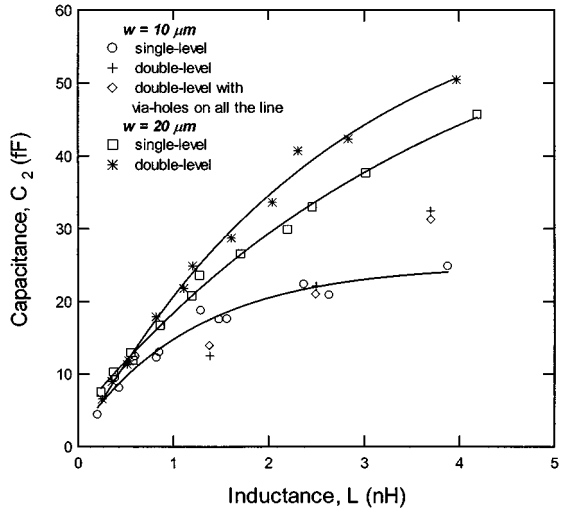

Fig. 10. Capacitance C_2 versus inductance of the fabricated 3-D silicon inductors.

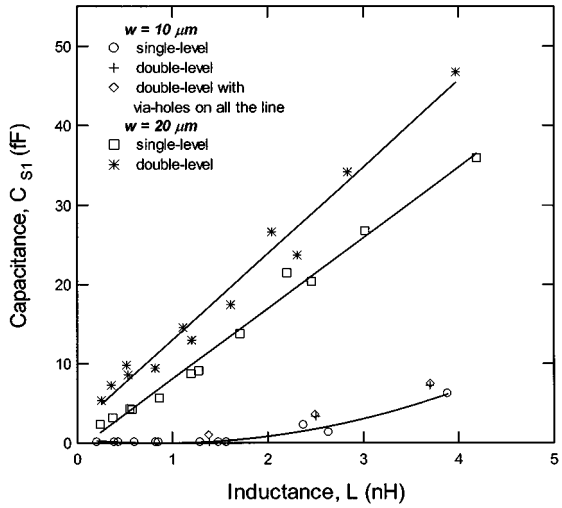

Fig. 11. Capacitance C_{S1} versus inductance of the fabricated 3-D silicon inductors.

where $\mathrm{Re}[Z_{\mathrm{in}}]$ is the real part of the input impedance of the inductor and $\mathrm{Im}[Z_{\mathrm{in}}]$ its imaginary part.

For high-frequency applications, a very high peak Q factor of 118.24 was measured at 53.6 GHz. The corresponding inductance is 0.39 nH. Higher value inductors also exhibit high-Q factor and good performance for the resonant frequency. A 1.38-nH spiral inductor exhibits a peak Q factor of 52.8 at 13.6 GHz with a resonant frequency as high as 24.7 GHz.

Compared to the state-of-the-art on-chip silicon inductors (see Fig. 13), the proposed 3-D inductors are more than competitive. The main competitors to 3-D silicon inductors, i.e., the promising micromachined inductors, are still too expensive and not yet reliable.

E. Guidelines for Optimum Design

The object of this section is to give some design elements for optimizing 3-D silicon inductors in terms of the quality factor. Two factors are investigated: the effect of the ground window surrounding the spiral pattern and the effect of the multilevel configuration.

As shown in Fig. 14 for the fabricated four-turn $w = 20$ μm 3-D silicon inductors, decreasing the gap G between the open ground window and the spiral pattern effectively improves the Q factor value with a shift toward higher frequency operation. This is mainly due to a reduction in the magnetic field that penetrates the conductive silicon substrate and generates eddy current. Moreover, note that reducing G also improves the loss characteristics of the 20-μm-wide TFMS line that forms the spiral pattern (see [21]). We expect that the limitation (of G) in terms of Q factor improvement should be of the order of a few micrometers due to coupling to the ground.

Compared to the single-level inductors, the four-turn $w = 20$ μm double-level inductors exhibit significantly higher Q factors (Fig. 14). This is the result of the improvement in the series resistance, which dominates the increase of parasitic capacitance for large inductors.

For smaller inductors, the fall in the series resistance with the double-level configuration is not enough to offset the increase in the parasitic capacitance. Therefore, as shown in Fig. 15, the

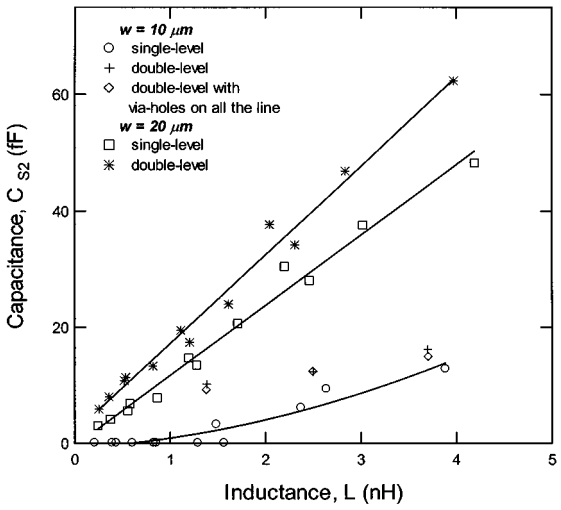

Fig. 12. Capacitance C_{S2} versus inductance of the fabricated 3-D silicon inductors.

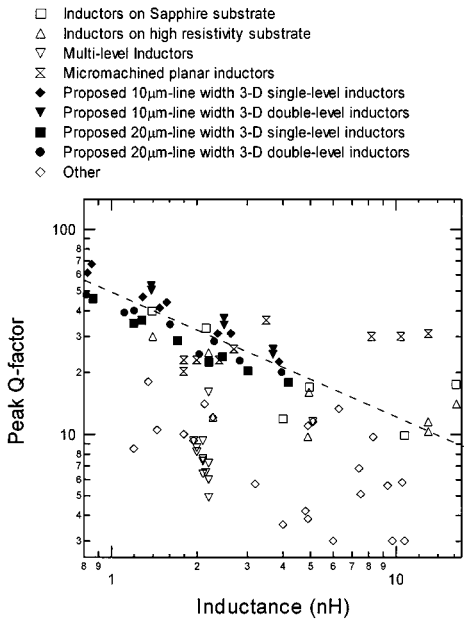

Fig. 13. State-of-the-art silicon on-chip inductors compared to the fabricated 3-D silicon inductors.

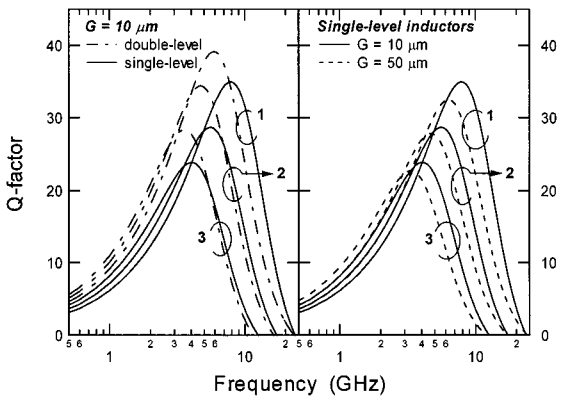

Fig. 14. Q factor of the fabricated $n = 4$, $w = 20\ \mu$m 3-D silicon inductors versus frequency and for different values of the internal diameter: 1-D $= 30\ \mu$m, 2-D $= 60\ \mu$m, and 3-D $= 100\ \mu$m.

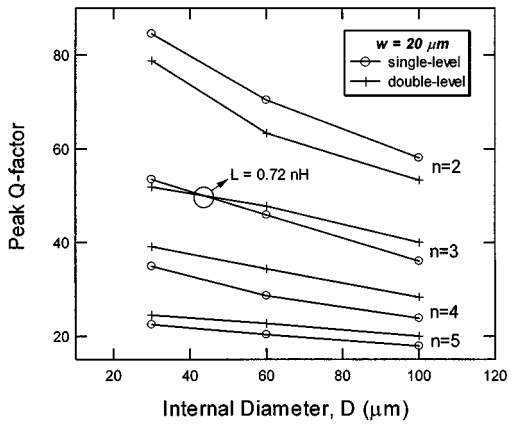

Fig. 15. Peak Q factor of the fabricated $w = 20\ \mu$m 3-D silicon inductors versus internal diameter D.

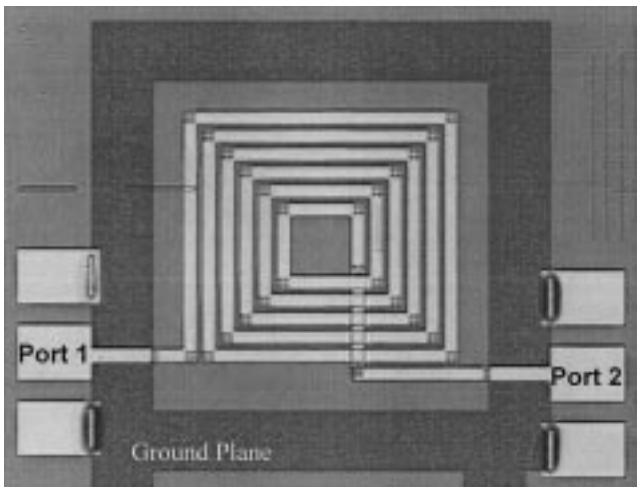

Fig. 16. 3-D GaAs six-turn double-level inductor: $w = 20\ \mu$m, $G = 50\ \mu$m, and $D = 100\ \mu$m.

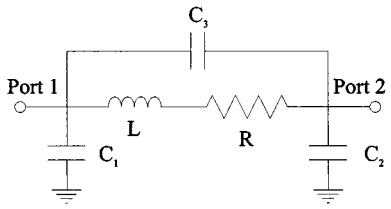

Fig. 17. Lumped-element equivalent circuit model of the 3-D GaAs inductors.

single-level configuration is more effective in terms of Q factor performance for small inductors. For 20-μm linewidth inductors, the cross point between the two configurations is estimated to 0.72 nH.

III. High-Q Factor GaAs 3-D Inductors

A. Structure and Principle

The structure of the proposed 3-D GaAs inductors is very similar to the previously detailed 3-D silicon inductors. The spiral pattern still consists of a 2-μm-thick top-level low-loss Au line of the 3-D process. A 1-μm-thick TFMS line located 2.5 μm under the spiral pattern is used as the inductor underpass. The open ground plane is formed on the lower-level Au

TABLE I
MODEL PARAMETERS OF 3-D GaAs INDUCTORS

Structure #	Dimensions (μm)			Lumped-element Equivalent Circuit Parameters					F_{res}	Peak Q
	W (μm)	D (μm)	n	L (nH)	R (Ω)	C_1 (pF)	C_2 (pF)	C_3 (pF)	(GHz)	
Single-level Inductors										
n6w20D20_S	20	20	6	5.275	3.802	0.084	0.0605	0.012	7.07	23.71
n6w20D60_S	20	60	6	6.80	4.418	0.094	0.0685	0.01	5.96	22.18
n6w20D100_S	20	100	6	8.81	5.449	0.105	0.0765	0.01	4.99	19.49
n4w10D20_S	10	20	4	1.106	2.069	0.0343	0.0171	0.000	25.82	33.39
n4w10D60_S	10	60	4	2.016	3.153	0.0375	0.0214	0.003	17.61	27.22
n4w10D100_S	10	100	4	2.936	4.156	0.0427	0.0298	0.000	14.21	24.27
Double-level Inductors										
n6w20D20_D	20	20	6	4.9	2.66	0.0794	0.1356	0.0	8.07	35.93
n6w20D60_D	20	60	6	6.46	3.192	0.0944	0.1506	0.0	6.44	31.53
n6w20D100_D	20	100	6	8.08	3.832	0.1094	0.1656	0.0	5.35	27.28

layer of the 3-D MMIC process, 10 μm under the spiral pattern, and just over the GaAs active process.

Note that the position of the ground plane under the spiral pattern and the low effective dielectric constant of the polyimide layer make the single-level inductor very similar to the coplanar waveguide GaAs inductor formed on semi-insulating substrate. Therefore, the peak Q factor of the fabricated inductors is expected to be comparable to those of GaAs coplanar inductors.

As for silicon 3-D inductors, the multilevel configuration can appreciably reduce the series resistance and increase the Q factor. Again, this effect is offset by an increase in the parasitic capacitance. Nevertheless, due to the use of a semi-insulating substrate and since the open ground plane surrounds the spiral pattern with a large gap, the increase in the parasitic capacitance is mainly due to the coupling between the lines and remains low. Therefore, for multilevel 3-D GaAs inductors, the reduction in the series resistance is the dominant effect and the Q factor should be significantly improved with the multilevel configuration.

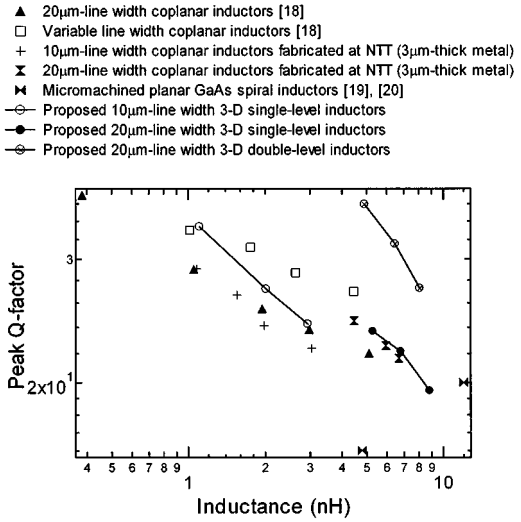

Fig. 18. State-of-the-art GaAs on-chip inductors compared to the fabricated 3-D GaAs inductors.

B. Fabrication and Experimental Results

The 3-D GaAs inductors were formed according to the 3-D process over an ordinary GaAs active device's process (0.15-μm pseudomorphic high electron-mobility transistor (HEMT) technology [22]). Fig. 16 shows an example of a 3-D GaAs double-level inductor as fabricated. The inductors have a constant line-to-line spacing s of 10 μm. The ground window surrounds the spiral pattern with a gap of 20 μm for $w = 10$ μm, and 50 μm for $w = 20$ μm. The GaAs substrate is 600-μm thick.

The inductors were characterized on-wafer from 0.5 to 20 GHz. The measurement of open- and shorted-pad reference circuits allowed the RF pads of the DUT to be deembedded. Fig. 17 shows the two-port lumped-element model of the inductors and Table I summarizes the model values extracted from the measurements of the fabricated inductors. For a 4.9-nH inductor, a very high peak Q factor of 35.93 is achieved at 4.66 GHz. The resonant frequency of this inductor is 8.07 GHz.

A comparison against the state-of-the-art on-chip GaAs inductors (see Fig. 18) shows that the proposed 3-D inductors in a single-level configuration exhibit comparable performance to coplanar GaAs inductors of equivalent size. In the double-level configuration, the proposed 3-D inductors exhibit very high peak Q factor, the highest yet reported for GaAs on-chip inductors.

C. Guidelines for Optimum Design

Fig. 19 shows the measured and simulated peak Q factors of single- and double-level 3-D GaAs inductors. The simulation was performed using Sonnet electromagnetic software for different numbers of turns. The measured results are in good agreement with the simulated results.

Fig. 19 gives some guidelines for the optimum design of the GaAs inductors. For single-level inductors, 10-μm linewidth inductors give the best results in terms of peak Q factor for inductances lower than 2.3 nH. For higher inductances, it is better to use 20-μm linewidth inductors.

Regarding the double-level configuration, the 20-μm linewidth inductors give better performance than the 10-μm linewidth inductors from the inductance of 0.8 nH and probably lower considering the shape of the simulation curve.

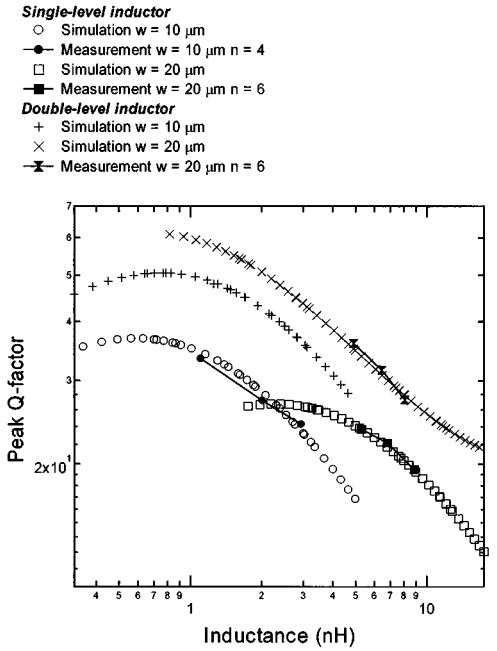

Fig. 19. Measured and simulated peak Q factor of the 3-D GaAs inductors versus inductance.

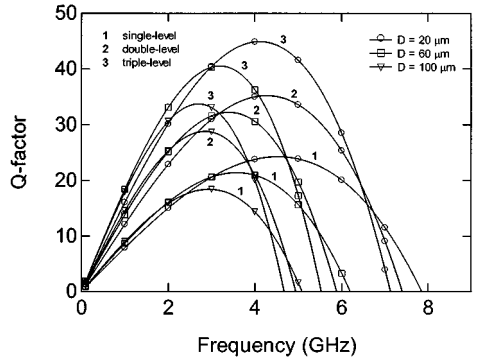

Fig. 20. Simulated Q factor of six-turn $w = 20$ μm, $G = 50$ μm, $s = 10$ μm 3-D GaAs inductors versus frequency in single-, double-, and triple-level configurations.

Compared to the single-level inductors, double-level inductors exhibit improved Q factors with comparable resonant frequency. This confirms that the factor determining the Q factor value for GaAs inductors is the series resistance of the line.

Therefore, it is expected that triple-level inductors will provide even higher peak Q factors. This is confirmed by the simulation of six-turn $w = 20$ μm, $G = 50$ μm, $s = 10$ μm 3-D GaAs inductors in single-, double-, and triple-level configurations (see Fig. 20). For these inductors, the inductance is slightly affected by the increase in the number of metal layers used to form the spiral pattern, but the series resistance is significantly improved. Thus, a peak Q factor as high as 44.92 at 4.11 GHz is expected for a 4.72-nH inductance. The corresponding resonant frequency of this inductor is expected to be 7.12 GHz.

IV. Conclusion

We have proposed a novel inductor topology that more fully utilizes the potential of the 3-D MMIC technology. Inductors implemented on both silicon conductive substrate and GaAs substrate have exhibited superior performance to state-of-the-art on-chip inductors.

Moreover, the performance limits of the proposed topology in terms of quality factor has been discussed and guidelines for optimum designs have been provided for both technologies.

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